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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,291	07/09/2003	Ik-Soo Choi	P68981US0	7044

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EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,291	CHOI ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/13/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 1, 2005 has been entered.

Claim Objections

Claim 10 is objected to because of the following informalities: in line 13, the examiner believes the word –that – should be inserted before "consists". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 4-11, and 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (AAPA, see specification pages 1-3 and Figure 1) in view of Nakao et al. (U.S. Patent No. 6,809,000).

In re claims 1 and 10, AAPA discloses the method of fabricating capacitor of semiconductor device, comprising the steps of:

forming sequentially a lower electrode (11) and a dielectric layer (12, see specification, page 1, line 23 through page 2, line 12) having high dielectric constant on semiconductor substrate which has gone through predetermined processes (see spec. page 2, lines 17-18);

forming a first metal layer (13A) on the dielectric layer;

forming a polysilicon layer (13B) on the first metal layer;

patterning the polysilicon layer and the first metal layer.

AAPA does not disclose the method of forming a second metal layer covering the patterned polysilicon layer and first metal layer and the semiconductor substrate, wherein a side wall of the patterned first metal layer is electrically connected to the second metal layer and patterning the second metal layer to thereby form an upper electrode constituted with the patterned second metal layer, the patterned polysilicon layer, and the patterned first metal layer.

Nakao et al. discloses the method of forming a second metal layer (17 or 27) covering an upper electrode pattern on an entire surface of semiconductor substrate wherein a side wall of the patterned upper electrode pattern is electrically connected to the second metal layer and forming an upper electrode constituted with the second

metal layer and patterning the second metal layer to thereby form an upper electrode constituted or consisting of the patterned second metal layer, and the upper electrode pattern (see Figure 1, 2, 3, 7(a-c) 9 (a-c) and column 8, line 59 through column 9, line 5, and column 10, line 24 through column 12, line 30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a second metal layer over the upper electrode of AAPA, such that an upper electrode constituted with the patterned second metal layer, the patterned polysilicon layer, and the patterned first metal layer is formed in order to form a diffusion barrier that allows for a higher breakdown voltage (see Nakao et al. column 3, lines 40-50 and column 9, line 50 through column 10, line 5).

The examiner notes that in the combined AAPA and Nakao et al. the second metal layer of Nakao et al. will be electrically connected with the patterned upper electrode pattern of the AAPA (13A 13B), including the sidewall of the first metal layer (13A), because the upper electrode layers are conductive without any insulating layers therebetween and thus all portions of all conductive layers of the upper electrode will be electrically connected.

In re claims 2 and 11, AAPA disclose the method as recited claim wherein titanium nitride (TiN) layer used for forming the first metal layer (13A).

In re claims 5 and 14, the combined AAPA and Nakao et al. disclose the method wherein the second metal layer is constituted with one of such layers as a titanium nitride (TiN) layer, a titanium (Ti) layer, a tungsten (W) layer and an aluminum (Al.) layer (see Nakao et al. 17, 27)

In re claims 8 and 17, AAPA discloses the method wherein the dielectric layer is constituted with one of such layers as a tantalum oxide, a titanium oxide, an aluminum oxide-tantalum oxide double layer, strontium titanium oxide layer and a piezoelectric translator layer (see specification page 1, line 23 through page 2, line 2 and page 2 lines 20-24).

In re claims 9 and 18, the combined AAPA and Nakao et al. disclose the method of forming an interlayer insulation (14 of AAPA and 14 or 24 of Nakao) on an entire surface of the semiconductor substrate after forming the upper electrode and forming a contact hole (16 of AAPA and see Figure 1, 2, and 3 of Nakao) exposing a portion of the upper electrode by etching the interlayer insulation film.

In re claims 4, 7, 13, and 16, neither the AAPA nor Nakao et al. disclose the thickness of the polysilicon and first and second metal layers therefore they do not disclose the method wherein a thickness of the TiN layer ranges from about 100 Å to about 500Å, wherein a thickness of the second metal layer ranges from about 100 Å to about 1000Å and wherein a thickness of the polysilicon layer ranges form about 300 Å to about 2500Å.

The examiner notes that Applicant does not teach that the thickness range of the first and second metal layers and polysilicon layer solve any stated problem or are for any particular purpose. Therefore, the thickness range lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the TiN, polysilicon, and second metal layers to the thickness of about 100 Å to about 500Å,

about 300 Å to about 2500Å, and about 100 Å to about 1000Å, respectively, since the invention would perform equally well when formed at different thicknesses to form a upper electrode with a diffusion barrier, and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

Claims 3 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (AAPA, see specification pages 1-3 and Figure 1) and Nakao et al. (U.S. Patent No. 6,809,000) in view of Wolf et al. (Silicon Processing for the VLSI Era, Volume 1- Process Technology, Second Edition, pages 216-219) .

In re claims 3 and 12, neither AAPA nor Nakao et al. disclose the method wherein the TiN layer is formed by performing a chemical vapor deposition (CVD) process. Wolf et al. disclose the method of forming a TiN layer by CVD. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the TiN layer of the combined AAPA and Nakao et al. with a CVD process since CVD TiN has highly conformal coverage.

Claims 4, 7, 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (AAPA, see specification pages 1-3 and Figure 1) and Nakao et al. (U.S. Patent No. 6,809,000) in view of Yasaitis et al. (EP 0472135 A1).

In re claims 4, 7, 13, and 16, neither the AAPA nor Nakao et al. disclose the thickness of the polysilicon and first and second metal layers therefore they do not disclose the method wherein a thickness of the TiN layer ranges from about 100 Å to about 500Å, and wherein a thickness of the polysilicon layer ranges from about 300 Å to about 2500Å.

Yasaitis et al. disclose the method of forming the TiN and polysilicon layers to the thickness of about 100 Å to about and about 300 Å to about 2500 Å, respectively (see column 3, lines 30-40). The examiner notes that about 600 Å could be considered about 500Å. Furthermore, about 3500 Å could read anywhere from 2800 to 4200 Å when allowing the word about to be plus or minus 10%. Applicants recitation of about 2500 Å with a plus or minus of 10% can range from 2000 to 3000 Å. Thus, Yasaitis et al. teaches an overlapping range of thickness for the polysilicon layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the TiN and the polysilicon electrode of the claimed thicknesses because as Yasaitis et al. teaches these thickness allow for a capacitor that has minimal free carrier depletion and allows for the advantage of an "etch stop" (see Yasaitis et al. column 4, lines 5-42). Further, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

Claims 1-2, 4-11, and 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (AAPA, see specification pages 1-3 and Figure 1) in view of Kirlin et al. (U.S. Patent No. 6,320,213).

In re claims 1 and 10, AAPA discloses the method of fabricating capacitor of semiconductor device, comprising the steps of:

forming sequentially a lower electrode (11) and a dielectric layer (12, see specification, page 1, line 23 through page 2, line 12) having high dielectric constant on semiconductor substrate which has gone through predetermined processes (see spec. page 2, lines 17-18);

forming a first metal layer (13A) on the dielectric layer;

forming a polysilicon layer (13B) on the first metal layer;

patterning the polysilicon layer and the first metal layer.

AAPA does not disclose the method of forming a second metal layer covering the patterned polysilicon layer and first metal layer and the semiconductor substrate, wherein a side wall of the patterned first metal layer is electrically connected to the second metal layer and patterning the second metal layer to thereby form an upper electrode constituted with the patterned second metal layer, the patterned polysilicon layer, and the patterned first metal layer.

Kirlin et al. discloses the method of forming a second metal layer (120, see column 6, lines 37-65) covering an upper electrode pattern on an entire surface of semiconductor substrate wherein a side wall of the patterned upper electrode pattern is electrically connected to the second metal layer and forming an upper electrode constituted or consisting of the second metal layer and patterning the second metal layer to thereby form an upper electrode constituted or consisting of the patterned second metal layer, and the upper electrode pattern (see Figure 8).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a second metal layer by the method of Kirlin et al. over the upper electrode of AAPA, such that an upper electrode constituted with the patterned second metal layer, the patterned polysilicon layer, and the patterned first metal layer is formed in order in order to form a diffusion barrier which prevents diffusion of oxygen and subsequent degradation of the upper electrode (see column 6, lines 37-65 and column 2, lines 1-20).

The examiner notes that in the combined AAPA and Kirlin et al. the second metal layer of Kirlin et al. will be electrically connected with the patterned upper electrode pattern of the AAPA (13A 13B), including the sidewall of the first metal layer (13A), because the upper electrode layers are conductive without any insulating layers therebetween and thus all portions of all conductive layers of the upper electrode will be electrically connected.

In re claims 2 and 11, AAPA disclose the method as recited claim wherein titanium nitride (TiN) layer used for forming the first metal layer (13A).

In re claims 5 and 14, the combined AAPA and Kirlin et al. disclose the method wherein the second metal layer is constituted with one of such layers as a titanium nitride (TiN) layer, a titanium (Ti) layer, a tungsten (W) layer and an aluminum (Al.) layer (see Kirlin 120)

In re claims 8 and 17, AAPA discloses the method wherein the dielectric layer is constituted with one of such layers as a tantalum oxide, a titanium oxide, an aluminum oxide-tantalum oxide double layer, strontium titanium oxide layer and a piezoelectric

translator layer (see specification page 1, line 23 through page 2, line 2 and page 2 lines 20-24).

In re claims 6 and 15, the combined AAPA and Kirlin et al. disclose the method of forming the thickness of the second metal layer ranges from about 100 Å to about 1000Å (approximately 100 nm; see column 6, lines 37-45)

In re claims 9 and 18, the combined AAPA and Kirlin et al. disclose the method of forming an interlayer insulation (14 of AAPA and 122 of Kirlin) on an entire surface of the semiconductor substrate after forming the upper electrode and forming a contact hole (16 of AAPA and 125 of Kirlin) exposing a portion of the upper electrode by etching the interlayer insulation film.

In re claims 4, 7, 13 and 16, neither the AAPA nor Kirlin et al. disclose the thickness of the polysilicon and first and second metal layers therefore they do not disclose the method wherein a thickness of the TiN layer ranges from about 100 Å to about 500Å, and wherein a thickness of the polysilicon layer ranges from about 300 Å to about 2500Å.

The examiner notes that Applicant does not teach that the thickness range of the first metal layers and polysilicon layer solve any stated problem or are for any particular purpose. Therefore, the thickness range lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the TiN and polysilicon layers to the thickness of about 100 Å to about 500 Å and about 300 Å to about 2500Å, respectively, since the invention would perform equally well when formed

at different thicknesses to form a upper electrode with a diffusion barrier, and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art (AAPA, see specification pages 1-3 and Figure 1) and Kirlin et al. (U.S. Patent No. 6,320,213) in view of Wolf et al. (Silicon Processing for the VLSI Era, Volume 1- Process Technology, Second Edition, pages 216-219) .

In re claim 3, neither AAPA nor Kirlin et al. disclose the method wherein the TiN layer is formed by performing a chemical vapor deposition (CVD) process. Wolf et al. disclose the method of forming a TiN layer by CVD. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the TiN layer of the combined AAPA and Kirlin et al. with a CVD process since CVD TiN has highly conformal coverage.

Claims 4, 7, 13, and 16, are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art (AAPA, see specification pages 1-3 and Figure 1) and Kirlin et al. (U.S. Patent No. 6,320,213) in view of Yasaitis et al. (EP 0472135 A1).

In re claims 4, 7, 13, and 16, neither the AAPA nor Kirlin et al. disclose the thickness of the polysilicon and first and second metal layers therefore they do not disclose the method wherein a thickness of the TiN layer ranges from about 100 Å to about 500Å, and wherein a thickness of the polysilicon layer ranges from about 300 Å to about 2500Å.

Yasaitis et al. disclose the method of forming the TiN and polysilicon layers to the thickness of about 100 Å to about and about 300 Å to about 2500 Å, respectively (see column 3, lines 30-40). The examiner notes that about 600 Å could be considered about 500Å. Furthermore, about 3500 Å could read anywhere from 2800 to 4200 Å when allowing the word about to be plus or minus 10%. Applicants recitation of about 2500 Å with a plus or minus of 10% can range from 2000 to 3000 Å. Thus, Yasaitis et al. teaches an overlapping range of thickness for the polysilicon layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the TiN and the polysilicon electrode of the claimed thicknesses because as Yasaitis et al. teaches these thickness allow for a capacitor that has minimal free carrier depletion and allows for the advantage of an "etch stop" (see Yasaitis et al. column 4, lines 5-42). Further, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

Response to Arguments

Applicant's arguments filed August 1, 2005 have been fully considered but they are not persuasive.

Applciants state that neither the combined AAPA and Nakao et al. nor the combined AAPA and Kirlin et al. disclose the method wherein the second metal layer covers the patterned polysilicon layer and the first metal layer and the semiconductor substrate wherein the side wall of the patterned first metal layer is electrically connected to the second metal layer. The examiner notes that in the combined AAPA and Nakao et al. the second metal layer of Kirlin et al. will be electrically connected with the patterned upper electrode pattern of the AAPA (13A 13B), including being electrically connected to the sidewall of the first metal layer (13A), because the upper electrode layers are conductive without any insulating layers therebetween and thus all portions of all conductive layers of the upper electrode will be electrically connected. Similarly, in the combined AAPA and Kirlin et al. the second metal layer of Kirlin et al. will be electrically connected with the patterned upper electrode pattern of the AAPA (13A 13B), including being electrically connected to the sidewall of the first metal layer (13A), because the upper electrode layers are conductive without any insulating layers therebetween and thus all portions of all conductive layers of the upper electrode will be electrically connected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Primary Examiner
Art Unit 2812

jmk